FM680

User Manual for Virtex-6 XMC card

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Revision History

Date	Revision	Version
December 15, 2009	First release	1.0
January 20, 2010	Minor modifications	1.1
April 23 2010	Corrected typos	1.2
August 16 2010	Corrected typos	1.3
August 17	Added image 10 for the JTAG connector location	1.4

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Acronyms and related documents

1.1 Acronyms

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DCI	Digitally Controlled Impedance
DDR	Double Data Rate
DSP	Digital Signal Processing
EPROM	Erasable Programmable Read-Only Memory
FBGA	Fineline Ball Grid Array
FPDP	Front Panel Data Port
FPGA	Field Programmable Gate Array
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LVTTL	Low Voltage Transistor Logic level
LVDS	Low Differential Data Signaling
LSB	Least Significant Bit(s)
LVDS	Low Voltage Differential Signaling
MGT	Multi-Gigabit Transceiver
MSB	Most Significant Bit(s)
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCI-e	PCI Express
PLL	Phase Locked Loop
PMC	PCI Mezzanine Card
QDR	Quadruple Data rate
SDRAM	Synchronous Dynamic Random Access memory
SRAM	Synchronous Random Access memory

Table 1: Glossary

1.2 Related Documents

- IEEE Std 1386.1-2001: IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC).
- ANSI/VITA 20-2001 : Conduction Cooled PMC.
- ANSI/VITA 42.0-2005: XMC Switched Mezzanine Card Auxiliary Standard.
- ANSI/VITA 42.3-2006: XMC PCI Express Protocol Layer Standard
- IEEE Std 1386-2001: IEEE Standard for a Common Mezzanine Card (CMC) Family.
- Xilinx Virtex-5 Documentation
- Xilinx Virtex-6 Documentation

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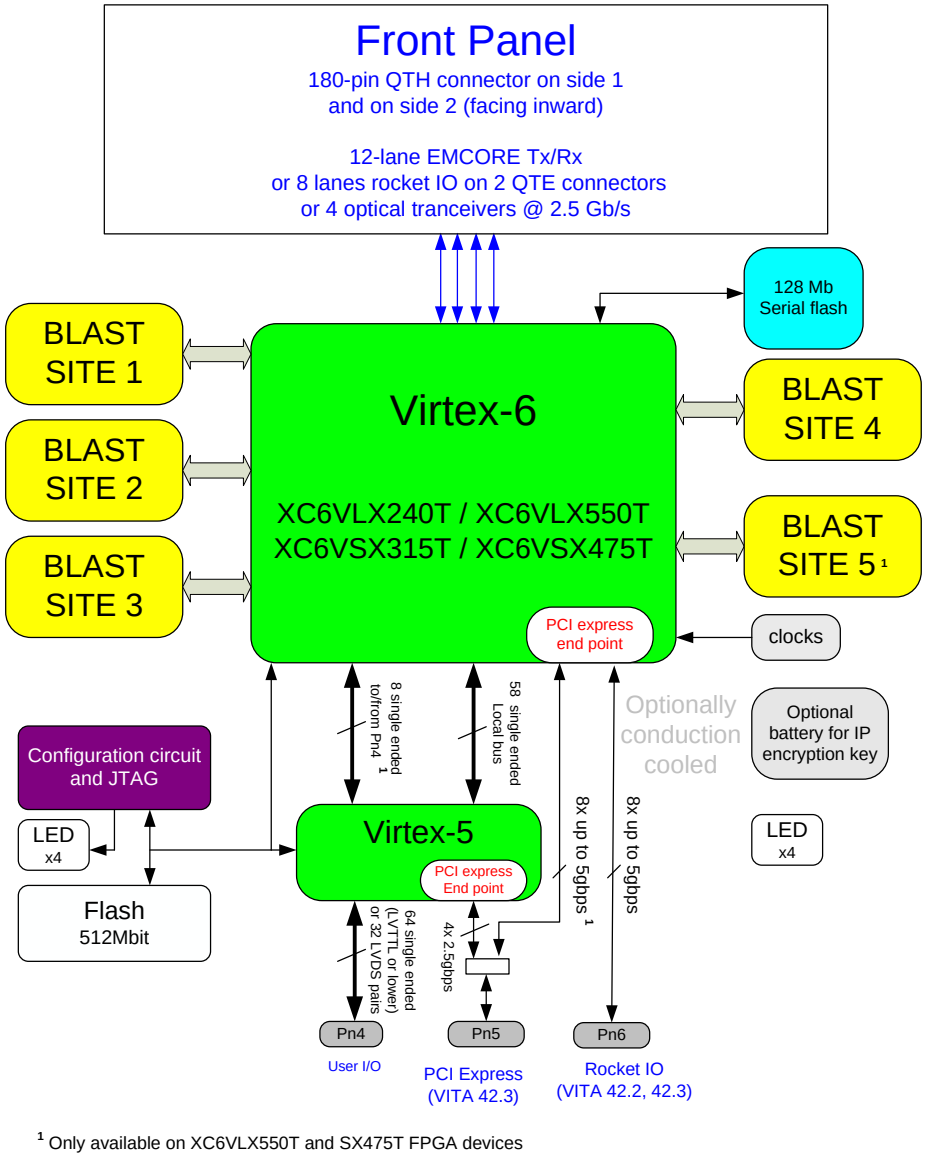
1.3 General description

The FM680 is a high performance XMC, optionally conduction cooled, dedicated to digital signal processing applications with high bandwidth and complex algorithms requirements. It offers various interfaces, fast on-board memory resources, one Virtex-5 FPGA with embedded PCI-express endpoint or Serial Rapid IO and one Virtex-6 device. It can be utilized, for example, to accelerate frequency-domain algorithms with off-the-shelf Intellectual Property cores for applications that require the highest level of performances. The FM680 is mechanically and electrically compliant to the standard and specifications listed in section 1.2 of this document. A top level diagram is depicted in Figure 1.



[1] Only available on XC6VLX550T and SX475T FPGA devices

Figure 1: FM680 block diagram

Build on the success of its predecessor boards of the FM48x series the FM680 also uses the BLAST technology. A total of 5 BLAST sites connect directly to the Virtex-6 FPGA.

BLAST, Board Level Advanced Scalable Technology, is a small PCB module that allows customization of the FM680 in memory extensions, processing units and communication interfaces. For more information about the available BLASTs on the FM680 please consult the following page: BLAST modules http://www.4dsp.com/BLAST.htm

2 Installation

2.1 Requirements and handling instructions

- The FM680 must be installed on a motherboard compliant to the VITA 42.3 standard.
- Do not flex the board
- Observe ESD precautions when handling the board to prevent electrostatic discharges.
- Do not install the FM680 while the motherboard is powered up.

2.2 Firmware and software

Drivers, API libraries and a program example working in combination with a pre-programmed firmware for both FPGAs are provided. The FM680 is delivered with an interface to the Xilinx PCI-e endpoint core in the Virtex-5 device as well as an example VHDL design in the Virtex-6 device so users can start performing high bandwidth data transfers over the PCI bus right out of the box. For more information about software installation and FPGA firmware, please refer the 4FM Get Started Guide.

3 Design

3.1 FPGA devices

The Virtex-5 and Virtex-6 FPGA devices interface to the various resources on the FM680 as shown on Figure 1. They also interconnect to each other via 58 general purpose pins including 4 clock pins (2 pairs, one in each direction, 100Ω terminated). A 16 bits single ended bus is also available between the two FPGA devices for communication with the Pn4 bus or general purpose communication.

3.1.1 Virtex-5 device family and package

The Virtex-5 device is from the Virtex-5 LX family. It can be either an XC5VLX20T or XC5VLX30T in a Fineline Ball Grid array with 323 balls (FF323).

3.1.2 Virtex-6 device family and package

The Virtex-6 device is dedicated to Digital Signal Processing, video processing or communication applications and can be chosen from the SXT or LXT family devices. Its package is based on Fineline Ball Grid array with 1759 balls. In terms of logic and dedicated DSP resources, the FPGA B can be chosen from the following types: LX240T, LX550T, SX315T and the SX475T (FF1759).

3.2 Inter-FPGA interface

The Virtex-5 device is connected to the Virtex-6 device using a 54 pin bus plus 2 differential clock signals. Also there are 16 single ended pins available that can be used as general

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purpose IO or as a connection to the Pn4 bus. Please be aware that 8 of those extra bits are available only on the SX475T and the LX550T FPGA types.

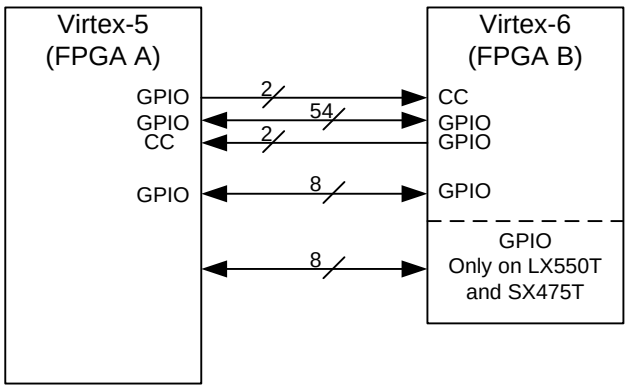

Figure 2: Inter-FPGA Interface

3.3 PCI-express architecture

The Virtex-5 device is connected to the XMC connector (P15) and offers a PCI Express® Endpoint block integrated in the FPGA. The endpoint will support a 4 lane PCI-express bus.

The following performances have been recorded with the FM680 transferring data on the bus:

- **PCIe 1 lane: 180Mbytes/s sustained**
- **PCIe 4 lanes: 600Mbytes/s sustained**

A PCI express switch will be used to optionally route the 4 lanes from the P15 connector to the Virtex-6 device. The remaining 4 transceiver lanes on the P15 connector will be routed to the Virtex-6 device as well.

Furthermore the VITA 42.3 standard defines an optional P16 connector which can carry an additional 8 lanes of PCI-express. All these lanes are routed to the Virtex-6 device directly. An overview of the PCI-express subsystem is shown in Figure 3.

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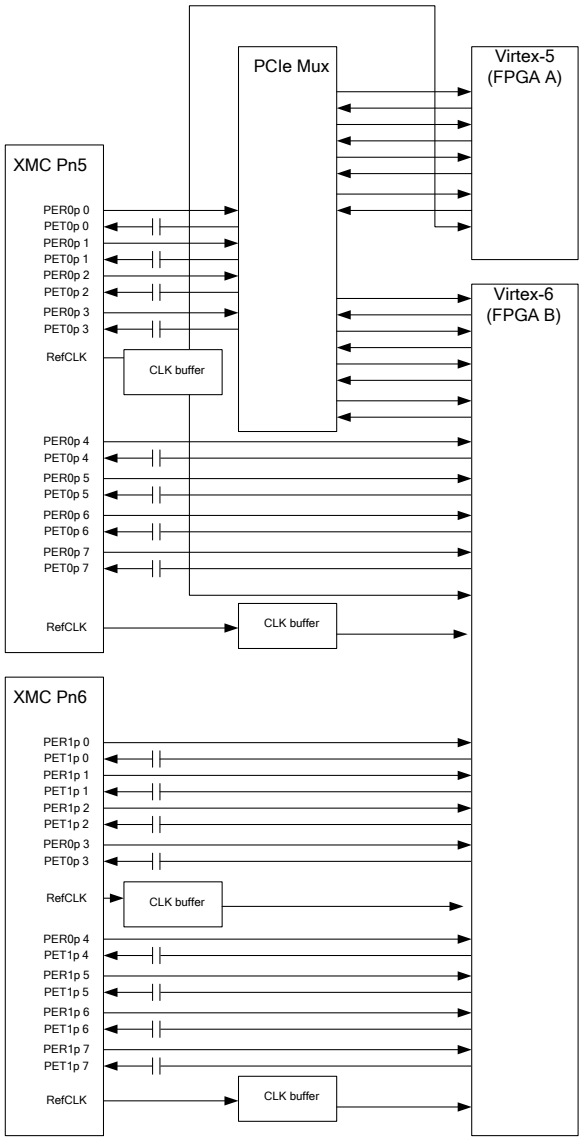

Figure 3: PCI-express subsystem diagram.

3.4 Pn4 user I/O connector

The Pn4 connector is connected to the Virtex-5 device.

Connector pin	Signal name	FPGA pin		FPGA pin	Signal name	Connector pin
1	Pn4_IO0	R1		T1	Pn4_IO1	2
3	Pn4_IO2	V1		U1	Pn4_IO3	4
5	Pn4_IO4	P2		P3	Pn4_IO5	6
7	Pn4_IO6	V2		V3	Pn4_IO7	8
9	Pn4_IO8	R2		T2	Pn4_IO9	10
11	Pn4_IO10	U4		U3	Pn4_IO11	12
13	Pn4_IO12	K12		L18	Pn4_IO13	14
15	Pn4_IO14	M11		K16	Pn4_IO15	16
17	Pn4_IO16	M14		M13	Pn4_IO17	18
19	Pn4_IO18	M16		M15	Pn4_IO19	20
21	Pn4_IO20	M10		N11	Pn4_IO21	22
23	Pn4_IO22	T17		T16	Pn4_IO23	24
25	Pn4_IO24	T12		R12	Pn4_IO25	26
27	Pn4_IO26	T18		U18	Pn4_IO27	28
29	Pn4_IO28	P10		N10	Pn4_IO29	30
31	Pn4_IO30	U16		U15	Pn4_IO31	32
33	Pn4_IO32	V18		V17	Pn4_IO33	34
35	Pn4_IO34	R10		R11	Pn4_IO35	36
37	Pn4_IO36	V16		V15	Pn4_IO37	38
39	Pn4_IO38	T11		U11	Pn4_IO39	40
41	Pn4_IO40	R14		T14	Pn4_IO41	42
43	Pn4_IO42	V10		U10	Pn4_IO43	44
45	Pn4_IO44	U14		T13	Pn4_IO45	46
47	Pn4_IO46	P12		P13	Pn4_IO47	48
49	Pn4_IO48	U13		V13	Pn4_IO49	50
51	Pn4_IO50	V12		V11	Pn4_IO51	52
53	Pn4_IO52	R17		R16	Pn4_IO53	54
55	Pn4_IO54	R15		P18	Pn4_IO55	56
57	Pn4_IO56	K14		P15	Pn4_IO57	58
59	Pn4_IO58	N18		N17	Pn4_IO59	60
61	Pn4_IO60	N16		N15	Pn4_IO61	62
63	Pn4_IO62	N13		N12	Pn4_IO63	64

Table 2 : Pn4 pin assignment

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3.5 Serial FLASH

A 128 Mbits serial flash device (S25FL128P) will be available to the Virtex-6 device. This flash allows the storage of vital data like processor boot code and settings into a non volatile memory.

The flash is operated using a standard SPI interface that can run up to 104 MHz, allowing for a page programming speed up to 208 KB/s. Reading data from the flash can be done at speeds up to 13 MB/s.

The SPI programming pins will be connected to a bank that supports 1V8, whereas the serial flash will be operating at 3V3. This will not cause problems for the signals from the Virtex-6 to the flash device but the signal from the flash device to the Virtex-6 will have to pass through a level translator (SN74AVC4T245).

3.6 BLAST sites

Thanks to the availability of 5 BLAST sites a wide variety of memory and processing modules can be connected to the Virtex-6 device. For each BLAST site it is possible to choose from the list of available BLAST modules.

For more information about the available BLASTs on the FM680 please consult the following page: BLAST modules http://www.4dsp.com/BLAST.htm

Table 3: BLAST Configuration Options

BLAST SITE	1	2	3	4	5(3)
Single BLAST	YES	YES	YES	YES	YES
Single Extended BLAST(1)	YES	YES	YES	YES	YES
Double BLAST(2)	YES	YES		YES	YES
Double Extended BLAST(1)(2)	YES	YES		YES	YES

1) Single and double extended BLAST placed in BLAST sites 4 and 5 will protrude 3mm from edge of the board.

2) BLAST SITES 1 and 2, 4 and 5 are paired when using double BLAST.

3) Only available on XC6VLX550T and SX475T FPGA devices

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Table 4: BLAST Memory/Processing Options

BLAST SITE	1	2	3	4	5(1)
DDR3	YES	YES	YES	YES	NO
DDR2	YES	YES	YES	YES	NO
QDR	YES	YES	YES	YES	YES
ADV212 JPEG2000	YES	YES	YES	YES	YES
32GB NAND FLASH	YES	YES	YES	YES	YES

1) Only available on XC6VLX550T and SX475T FPGA devices

Due to its small form factor and ease of design, the BLAST modules enable a rapid solution for custom memory or processing requirements.

3.7 External IO interfaces

The Virtex-6 device interfaces to the front panel daughter card on the FM680 via a high speed connector. 174 I/Os are available from the FPGA to/from the daughter card that can be mounted in the IO area defined by the XMC standard. Figure .. depicts the mechanical set-up for the IO area daughter card option.

3.7.1 Front Panel daughter card

(Only available with front panel daughter card purchase and not in combination with the optical transceivers or EMCORE)

The Virtex-6 device interfaces to a 180-pin connector placed in the Front panel I/O area (on both side 1 of the PCB). It serves as a base for a daughter card and offers I/O diversity to the FM680 PMC. The FPGA I/O banks are powered either by 1.8V or 2.5V via a large 0 ohms resistor (2.5V is the default if not specified otherwise at the time of order). Using the Xilinx DCI termination options to match the signals impedance allows many electrical standards to be supported by this interface. The VRN and VRP pins on the I/O banks connected to the daughter card connector are respectively pulled up and pulled down with 50Ω resistors in order to ensure optimal performances when using the Xilinx DCI options. The VREF pins are connected to 0.9V for DDR2 DCI terminations. Please, contact 4DSP Inc. for more information about available daughter card types.

The 180-pin Samtec connector pin assignment is as follows. All signals shown as LVDS pairs in the table can also be used for any standard that does not breach the electrical rules of the Xilinx I/O pad. The FP_Xi signals in the table below are routed as single ended.

Connector pin	Signal Name	FPGA pin		FPGA pin	Signal name	Connector pin
1	FP_P0	J12		A16	FP_P1	2
3	FP_N0	J11		B16	FP_N1	4
5	FP_X0	C13		D12	FP_X1	6
7	FP_P2(2)	M13		J13	FP_P3	8

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9	FP_N2[2]	N13		K13	FP_N3	10
11	FP_X2	K14		L14	FP_X3	12
13	FP_P4	H13		D16	FP_P5	14
15	FP_N4	G12		C16	FP_N5	16
17	FP_X4	H15		G14	FP_X5	18
19	FP_P6	F12		D13	FP_P7	20
21	FP_N6	E12		E13	FP_N7	22
23	FP_X6	E15		F15	FP_X7	24
25	FP_P8	B14		A15	FP_P9	26
27	FP_N8	C14		A14	FP_N9	28
29	FP_X8	C15		D15	FP_X9	30
31	FP_P10[2]	M14		M16	FP_P11	32
33	FP_N10[2]	N14		N15	FP_N11	34
35	FP_X10	H14		G13	FP_X11	36
37	FP_P12	A17		L16	FP_P13	38
39	FP_N12	B17		L15	FP_N13	40
41	FP_X12	J16		H16	FP_X13	42
43	FP_P14	D18		K17	FP_P15	44
45	FP_N14	C18		J17	FP_N15	46
47	FP_X14	M18		N18	FP_X15	48
49	FP_P16[2]	N16		L12	FP_P17[1]	50
51	FP_N16[2]	P16		M12	FP_N17[1]	52
53	FP_X16	K18		J18	FP_X17	54
55	FP_P18[1]	E14		H18	FP_P19	56
57	FP_N18[1]	F14		G18	FP_N19	58
59	FP_X18	G16		F16	FP_X19	60

Table 5 : Front Panel IO daughter card pin assignment Bank A

[1] Connected to a global clock pin on the FPGA. LVDS output not supported.

[2] Connected to a regional clock pin on the FPGA. LVDS output not supported.

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Connector pin	Signal Name	FPGA pin		FPGA pin	Signal name	Connector pin
61	FP_P20	G19		E19	FP_P21	62
63	FP_N20	F19		E18	FP_N21	64
65	FP_X20	C19		B19	FP_X21	66
67	FP_P22	F17		B18	FP_P23	68
69	FP_N22	G17		A19	FP_N23	70
71	FP_X22	J15		K15	FP_X23	72
73	FP_P24(2)	P18		G23	FP_P25	74
75	FP_N24(2)	P17		H23	FP_N25	76
77	FP_X24	D17		E17	FP_X25	78
79	FP_P26	B24		C24	FP_P27	80
81	FP_N26	A24		C23	FP_N27	82
83	FP_X26	G22		F22	FP_X27	84
85	FP_P28	B23		H21	FP_P29	86
87	FP_N28	B22		J21	FP_N29	88
89	FP_X28	F21		E22	FP_X29	90
91	FP_P30	E24		C21	FP_P31	92
93	FP_N30	E23		D21	FP_N31	94
95	FP_X30	H20		G21	FP_X31	96
97	FP_P32	K20		A22	FP_P33	98
99	FP_N32	L20		A21	FP_N33	100
101	FP_X32	D23		D22	FP_X33	102
103	FP_P34	B21		J22	FP_P35(2)	104
105	FP_N34	A20		K22	FP_N35(2)	106
107	FP_X34	J20		H19	FP_X35	108
109	FP_P36(2)	L22		L21	FP_N36(2)	110
111	3.3V/2.5V/1.8V				Vbatt (3)	112
113	FP_X36	K19		L19	FP_X37	114
115	3.3V/2.5V/1.8V				0.9V	116
117	3.3V/2.5V/1.8V				3.3V/2.5V/1.8V	118
119	FP_X38	F32		F31	FP_X39	120

Table 6: **Front Panel IO daughter card pin assignment Bank B**

(1) Connected to a global clock pin on the FPGA. LVDS output not supported.

(2) Connected to a regional clock pin on the FPGA. LVDS output not supported.

(3) Vbatt is connected to both Virtex-5 devices Vbatt pin.

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Connector pin	Signal Name	FPGA pin		FPGA pin	Signal name	Connector pin
121	FP_P37	E32		C20	FP_P38	122
123	FP_N37	D32		D20	FP_N38	124
125	FP_X40	E35		D35	FP_X41	126
127	FP_P39	B33		A32	FP_P40	128
129	FP_N39	C33		B32	FP_N40	130
131	FP_X42	G33		G32	FP_X43	132
133	FP_P41	H31		A34	FP_P42	134
135	FP_N41	G31		A35	FP_N42	136
137	FP_X44	D33		E33	FP_X45	138
139	FP_P43	L29		B34	FP_P44	140
141	FP_N43	L30		C34	FP_N44	142
143	FP_X46	J32		J31	FP_X47	144
145	FP_P45(1)	A36		M28	FP_P46	146
147	FP_N45(1)	B36		M29	FP_N46	148
149	FP_X48	K29		K30	FP_X49	150
151	FP_P47	H30		C35	FP_P48	152
153	FP_N47	J30		C36	FP_N48	154
155	FP_X50	AH31		AG31	FP_X51	156
157	FP_P49	D36		E34	FP_P50	158
159	FP_N49	D37		F34	FP_N50	160
161	FP_X52	AH29		AG29	FP_X53	162
163	FP_P51	T30		AG32	FP_P52	164
165	FP_N51	R30		AF31	FP_N52	166
167	FP_X54	AH30		AJ30	FP_X55	168
169	FP_P53(2)	N33		R32	FP_P54	170
171	FP_N53(2)	P33		T32	FP_N54	172
173	FP_X56	V31		W31	FP_X57	174
175	FP_P55(1)	AD31		AK33	FP_P56	176
177	FP_N55(1)	AD30		AJ32	FP_N56	178
179	FP_X58	AJ31		AK30	FP_X59	180

Table 7 : Front Panel IO daughter card pin assignment Bank C

3.7.2 Power connection to the front panel I/O daughter card

The Front Panel I/O daughter card on side 1 of the PCB is powered via a 7-pin connector of type BKS (Samtec). Each pin can carry up to 1.5A. The power connector's pin assignment is as follows.

Pin #	Signal	Signal	Pin #
1	+3.3V	+3.3V	2
3	+5V	GND	4
5	+12V	GND	6
7	-12V		

Table 8: Daughter card power connector pin assignment on PMC side 1

3.7.3 Front Panel optical transceivers

(Special build option and not in combination with the front panel daughter card or EMCORE)

Four 2.5 GB/s optical transceivers (LTP-ST11M) are available on the FM680 in the front panel area. They are connected to the MGT I/Os of the Virtex-6. Infiniband protocols as well as Gigabit Ethernet and Fibre channel (sFPDP) can be implemented over the transceivers. Lower rate optical transceivers (2.125 GB/s and 1.0625 GB/s) are available in the same form factor.

3.7.4 8 channels rocket IO on QTE connectors

(This is a special build option and not in combination with the optical transceivers or EMCORE)

Eight Rx/Tx Multi Gigabit Transceivers connected to the Virtex-6 are available in the front panel area on two connectors of type QTE. These connectors provide a base for a daughter card dedicated to high bandwidth communication via optical transceivers or copper (please refer to the FM489 web page for more details about available daughter cards). Infiniband protocols as well as Gigabit Ethernet, OC48 and Fibre channel (sFPDP) can be implemented over the transceivers. Eight LVTTL signals (four per connector) are also available for daughter card control.

Pin #	Signal	Signal	Pin #		Pin #	Signal	Signal	Pin #
1	Rx p3/7	+3.3V	2		15	Tx n2/6	CTRL3/7	16
3	Rx n3/7	+3.3V	4		17	Rx p1/5	GND	18
5	Tx p3/7	+3.3V	6		19	Rx n1/5	GND	20
7	Tx n3/7	+3.3V	8		21	Tx p1/5	GND	22
9	Rx p2/6	CTRL0/4	10		23	Tx n1/5	GND	24
11	Rx n2/6	CTRL1/5	12		25	Rx n0/4	Tx n0/4	26
13	Tx p2/6	CTRL2/6	14		27	Rx p0/4	Tx p0/4	28

Table 9: QTE connector pinout.

3.7.5 Emcore connector

(This is a special build option and not in combination with the optical transceivers or front panel daughter card)

Another front panel possibility is the 12 lanes Emcore connector (FM680V2). This connector comes with a TX and an RX version. FM680 will come with one TX and one RX connector. All the high speed serial connections will connect directly to the Virtex-6 FPGA.

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Part of the Emcore connector will protrude outside of front panel because the Emcore package dimensions are in breach of the XMC specifications in terms of height.

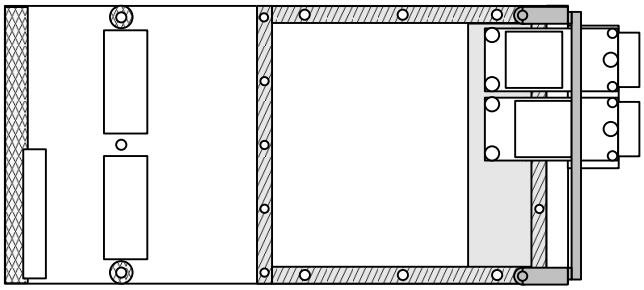

Figure 4: Emcore connectors protruding from front panel

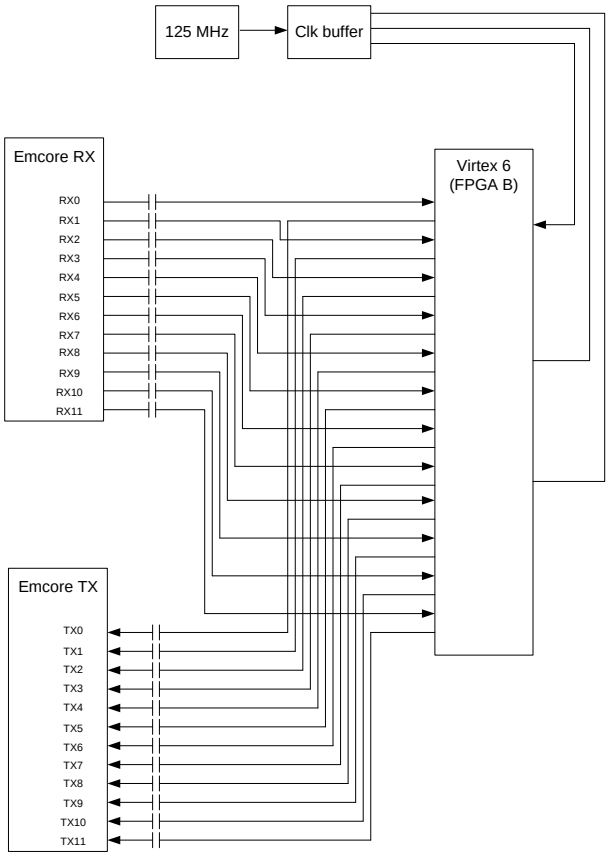

Figure 5: Emcore GTP connections

3.8 FPGA LED

Four LEDs are connected to the Virtex-5 device. In the default FPGA firmware, the LEDs are driven by the Virtex-6 device via the inter-FPGA interface.

The LEDs are located on side 2 of the PCB in the front panel area.

Figure 6: FPGA LED locations

3.9 FPGA configuration

3.9.1 Flash storage

The FPGA firmware is stored on board in a flash device. The 512Mbit device is partly used to store the configuration for both FPGAs. In the default CPLD firmware configuration, the Virtex-5 device and the Virtex-6 device are directly configured from flash if a valid bit stream is stored in the flash for each FPGA. The flash is pre-programmed in factory with the default firmware example for both FPGAs.

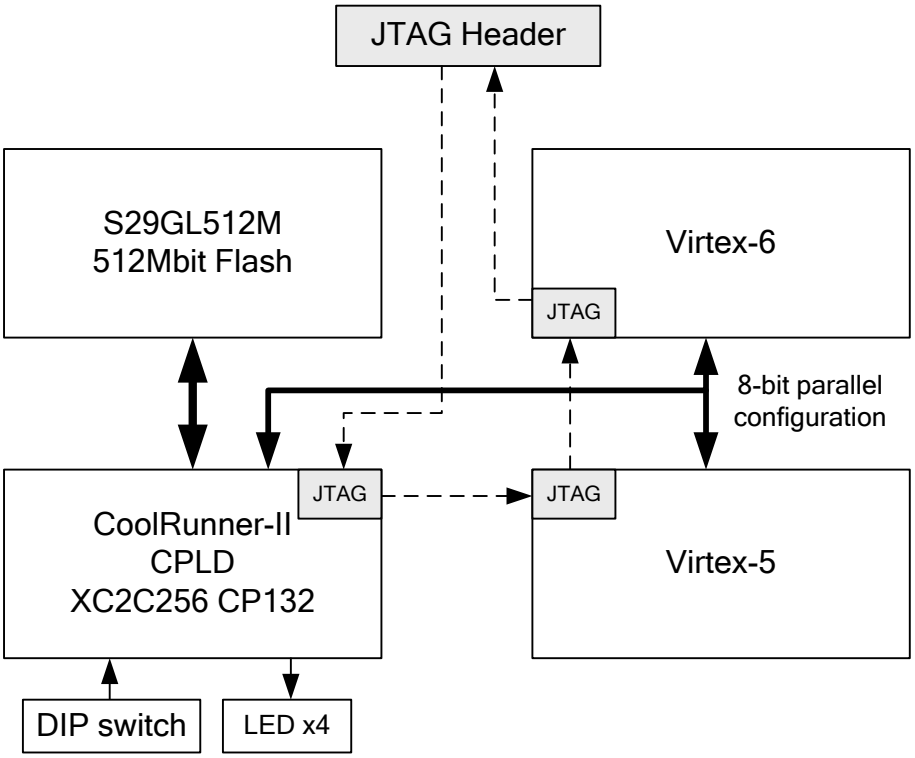

Figure 7 : Configuration circuit

3.9.2 CPLD device

As shown on Figure 7, a Cool Runner-II CPLD is present on board to interface between the flash device and the FPGA devices. The CPLD is used to program and read the flash. The data stored in the flash is transferred from the host motherboard via the PCI-express bus to the Virtex-5 device and then to the CPLD that writes the required bit stream to the storage device. A 31.25 MHz clock connects to the CPLD and is used to generate the configuration clock sent to the FPGA devices. At power up, if the CPLD detects that an FPGA configuration bit stream is stored in the flash for both FPGA devices, it will start programming the devices in SelecMap mode.

Do NOT reprogram the CPLD without 4DSP's approval

The CPLD configuration is achieved by loading with a Xilinx download cable a bit stream from a host computer via the JTAG connector. The FPGA devices configuration can also be achieved via the JTAG chain.

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3.9.2.1 DIP Switch

A switch (J1) is located next to the JTAG programming connector (J6) see Figure 8. The switch positions are defined as follows:

Figure 8: switch (J1) location

Sw1	**OFF**	Default setting. The Virtex-5 device configuration is loaded from the flash at power up.
	ON	Virtex-5 device safety configuration loaded from the flash at power up. To be used only if the Virtex-5 device cannot be configured or does not perform properly with the switch in the OFF position.
Sw2		Reserved
Sw3		Reserved
Sw4		Reserved

Table 10: Switch description

3.9.2.2 LED and board status

Four LEDs connect to the CPLD and give information about the board status.

LED 0	**Flashing**	FPGA A or B bit stream or user_ROM_register is currently being written to the flash
	ON	FPGA A not configured
	OFF	FPGA A configured
LED 1	**Flashing**	FPGA A or B bit stream or user_ROM_register is currently being written to the flash
	ON	FPGA B not configured
	OFF	FPGA B configured
LED 2	**Flashing**	The Virtex-5 device has been configured with the safety configuration bit stream programmed in the flash at factory. Please write a valid Virtex-5 device bit stream to the flash.
	ON	Flash is busy writing or erasing
	OFF	Flash device is not busy
LED 3	**ON**	CRC error. Presumably a wrong or corrupted FPGA bit stream has been written to the flash. Once on this LED remains on
	OFF	No CRC error detected

Table 11: LED board status

Figure 9: CPLD LED locations

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3.9.3 JTAG

A JTAG connector is available on the FM680 for configuration purposes. The JTAG can also be used to debug the FPGA design with the Xilinx Chipscope. A press fit connector is delivered with the board that can be plugged into the connector holes.

The JTAG connector can be placed on both sides of the PCB. The connector location seen from the bottom of the PCB is shown in Figure 10.

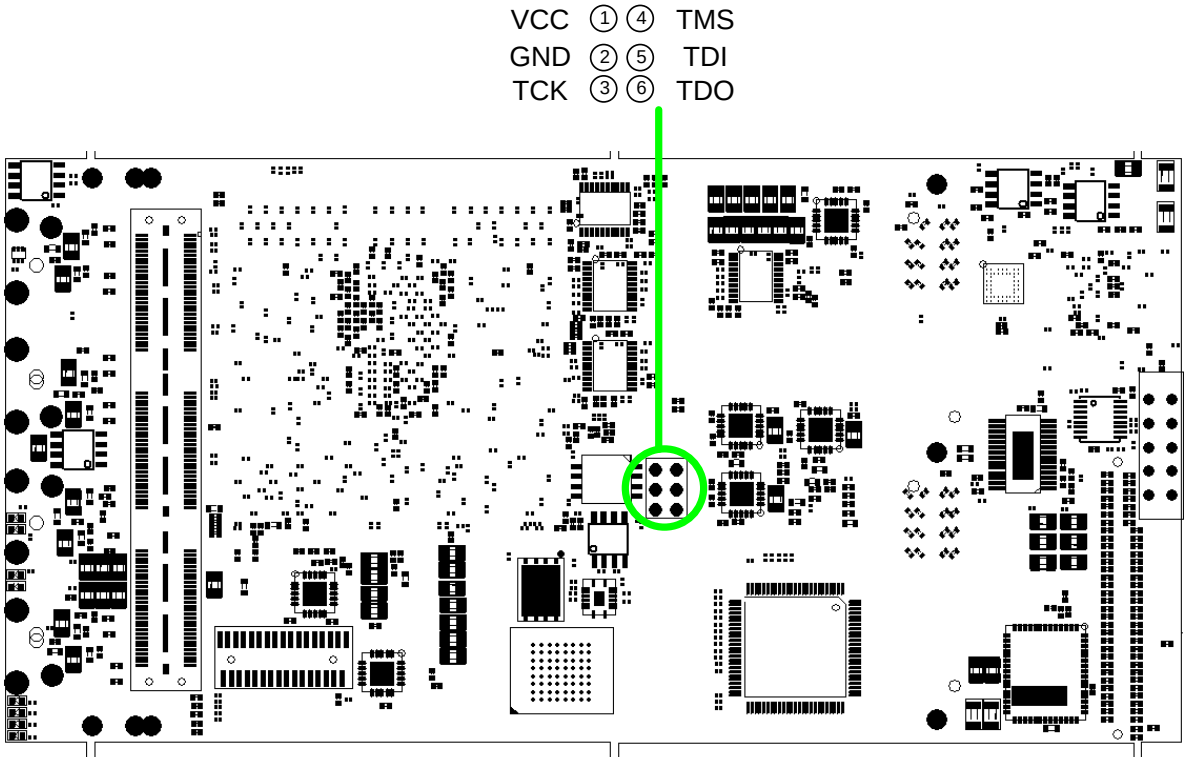

Figure 10: JTAG connector (J6) location

The JTAG connector pinout is as follows:

Pin #	Signal	Signal	Pin #
1	1.8V	TMS	4
2	GND	TDI	5
3	TCK	TDO	6

Table 12 : JTAG pin assignment

3.10 Clock tree

The FM680 clock architecture offers an efficient distribution of low jitter clocks.

Both FPGA devices receive a low jitter 125MHz clock. A low jitter programmable clock able to generate frequencies from 62.5MHz to 255.5MHz in steps of 0.5MHz is also available. This clock management approach ensures maximum flexibility to efficiently implement multi-clock domains algorithms and use the memory devices at different frequencies. Both clock

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buffer devices (CDCV1804) and the frequency synthesizer (CDCE925) are controlled by the Virtex-5 device.

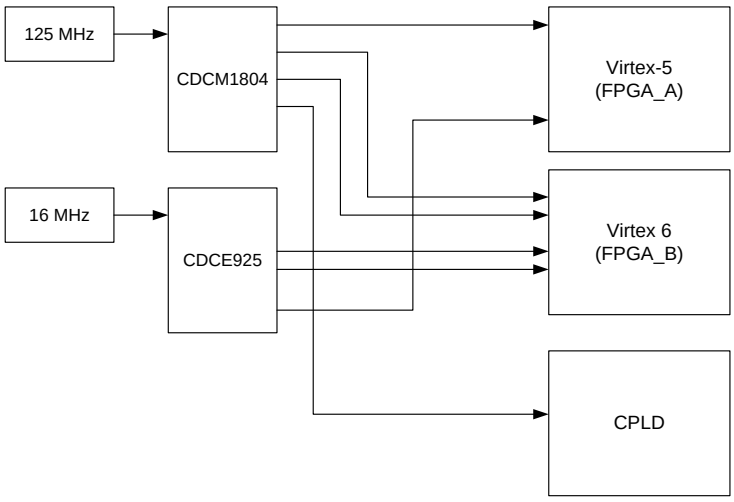

Figure 11 : Clock tree

4 Power requirements

The Power is supplied to the FM680 via the XMC Pn5 connector. Several DC-DC converters generate the appropriate voltage rails for the different devices and interfaces present on board.

The FM680 power consumption depends mainly on the FPGA devices work load. By using high efficiency power converters, all care has been taken to ensure that power consumption will remain as low as possible for any given algorithm.

After power up, the FM680 typically consumes 6 Watts of power. For precise power measurements it is recommended to use the Xilinx power estimation tools for both the Virtex-5 and Virtex-6 FPGA devices. The maximum current rating given in the table below is the maximum current that can be drawn from each voltage rail in the case resources are used to their maximum level.

Special precautions need to be taken to support the XMC VPOWER input, since the XMC standard dictates that this power supply can either be 12V or 5V. To overcome this, a voltage detection circuit detects whether VPOWER is 12V or 5V and enables a switching regulator or a Field Effect Transistor (FET). If VPOWER is 12V the switching regulator converts down to 5V otherwise the FET allows 5V to pass through.

Device/Interface	Voltage	Maximum current rating
DCI and memory reference voltage	0.9V	6 A
Virtex-6 device core	1.0V	10 A
Virtex-5 device core	1.0V	2 A
BLAST core and IO,Virtex-6 I/O banks	1.8V	6A

Virtex-5 device I/O bank connected to the front panel daughter card	0.9/1.0/1.8/2.5/3.3V	…A
front Panel I/O daughter card	5V	1A
Front Panel IO daughter card	3V3	3A
Front Panel IO daughter card	12V	1A
Front Panel IO daughter card	-12V	1A
MGT power supply	1.0V, 1.2V, 2.5V	2.0A, 2.5A, 0.01A respectively

Table 13 : Power supply

Optionally, the FM680 can be used as a stand alone module and is powered via the external power connector.

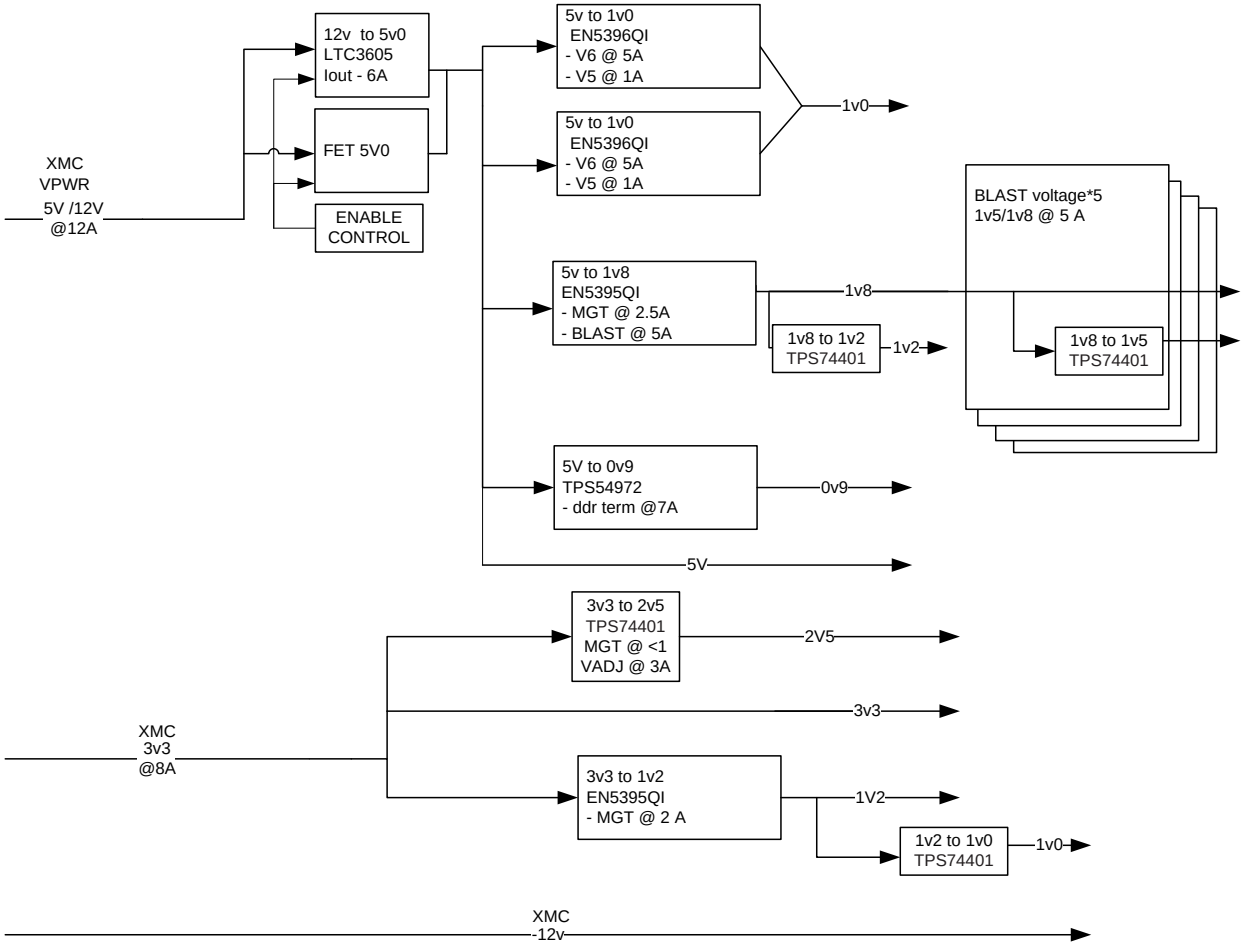

Figure 12 : Power supply

An ADT7411 device is used to monitor the power on the different voltage rails as well as the temperature. The ADT7411 data are constantly passed to the Virtex-6 device. Measurements can be accessed from the host computer via the PCI bus. A software utility delivered with the board allows the monitoring of the voltage on the 2.5V, 1.8V, 1.2V, 1.0V and 0.9V rails. It also displays both FPGAs junction temperature.

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4.1 External power connector for stand alone mode

An external power connector (J2) is available on side 2 of the PMC, next to the PMC connectors. It is used to power the board when it is in stand alone mode. This is a right angled connector and it will be mounted on board only if the card is ordered as a stand alone version (FM680-SA). The height and placement of this connector on the PCB breaches the PMC specifications and the module should not be used in an enclosed chassis compliant to PMC specifications if the external power connector is present on board.

Do not connect an external power source to J2 if the board is powered via the PMC connectors. Doing so will result in damaging the board.

The external power connector is of type Molex 43045-1021. Each circuit can carry a maximum current of 5A. The connector pin assignment is as follows:

Pin #	Signal	Signal	Pin #
1	3.3V	3.3V	2
3	5V	5V	4
5	GND	GND	6
7	GND	GND	8
9	-12V	12V	10

Table 14 : External power connector pin assignment

WARNING:

UNREGULATED UNPROTECTED EXTERNAL POWER SUPPLY CONNECTION

This board is designed with an UNSUPPORTED feature for an external power connector labeled as J2. Mounting a connector on the PCB breaches the PMC electrical and mechanical specifications of the PMC standard. This is a FACTORY ONLY feature that is used in the manufacturing process when powering the board is required in an UN-MOUNTED PCI bus mode, thus in stand alone mode. DO NOT connect an external power source to J2, doing so may result in damaging the board and will automatically VOID WARRANTY. Consult factory for further information.

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5 Environment

5.1 Temperature

Operating temperature

- 0°C to +60°C (Commercial)
- -40°C to +85°C (Industrial)

Storage temperature:

- -40°C to +120°C

5.2 Convection cooling

600LFM minimum

5.3 Conduction cooling

The FM680 can optionally be delivered as conduction cooled PMC. The FM680 is compliant to ANSI/VITA 20-2001 standard for conduction cooled PMC.

6 Safety

This module presents no hazard to the user.

7 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

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8 Technical support

Technical support for all 4DSP Product, hardware, software and firmware is available under 4DSP Terms and Conditions of Sales ONLY in its original condition AS-SHIPPED unless agreed to by 4DSP and documented in writing, prior to any modifications.

Terms and Conditions are available from http://www.4dsp.com/TCs.txt

Technical support requests should be sent to support@4dsp.com

Any electrical connections made to the board or other components shall be made only with approved connectors as specifically identified in the products official documentation.

Any modification to hardware including but not limited to removing of components, soldering or other material changes to in part or in whole to the PCM and/or its components will immediately invalidate and make void any warranty or extended support if any.

Further, and changes or modifications to software and/or firmware supplied with the Product, unless provided for in the Products official documentation, shall immediately invalidate and make void any warranty or extended support if any.

9 PCB revisions

10 Warranty

	Hardware	*Software/Firmware*
Basic Warranty (included)	1 Year from Date of Shipment	90 Days from Date of Shipment
Extended Warranty (optional)	2 Years from Date of Shipment	1 Year from Date of Shipment

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